IN THE CLAIMS:

Please amend the claims as set forth below.

1-34 (Cancelled).

35. (New) A distributed simulation system comprising:

a plurality of nodes, each of the plurality of nodes configured to simulate one of a plurality of electronic components of an electronic system under test, wherein the plurality of nodes are configured to communicate during a simulation using a predefined grammar that includes transmit signal message packets, wherein a transmit signal message packet comprises signal values corresponding to electronic signals in the electronic system under test, the electronic signals providing communication between the plurality of electronic components included in the electronic system under test;

wherein a first node of the plurality of nodes is assigned a first electronic component of the plurality of electronic components for the distributed simulation, and wherein the first node comprises the first electronic component implemented in hardware circuitry, and wherein the first node further comprises code to interface to the hardware circuitry to provide input signal values received from other nodes of the plurality of nodes to the hardware circuitry and to capture output signal values driven by the hardware circuitry to provide the output signal values to other nodes of the plurality of nodes; and

wherein a second node of the plurality of nodes simulates a second electronic component of the plurality of electronic components using a first simulation mechanism that does not include hardware circuitry that implements the second electronic component.

36. (New) The distributed simulation system as recited in claim 35 wherein the first simulation mechanism comprises a first simulator and a first model of the second electronic component.

37. (New) The distributed simulation system as recited in claim 36 wherein the first model is a register-transfer level model of the second electronic component.

38. (New) The distributed simulation system as recited in claim 36 wherein the first model is a behavioral level model of the second electronic component.

39. (New) The distributed simulation system as recited in claim 36 wherein the first model is a hardware verification language model of the second electronic component.

40. (New) The distributed simulation system as recited in claim 36 wherein the first model is described in a hardware description language that supports constructs for verification and an interface to one or more programming languages.

41. (New) The distributed simulation system as recited in claim 35 wherein the first simulation mechanism comprises one or more programs which, when executed, model the second electronic component.

42. (New) The distributed simulation system as recited in claim 41 wherein the one or more programs are coded in a programming language and compiled for execution.

43. (New) The distributed simulation system as recited in claim 42 wherein the programming language is C.

44. (New) The distributed simulation system as recited in claim 42 wherein the programming language is C++.

45. (New) The distributed simulation system as recited in claim 42 wherein the programming language is a portable, object-oriented language.

46. (New) The distributed simulation system as recited in claim 35 wherein the first simulation mechanism includes an emulator configured to emulate the second electronic component using one or more programmable logic devices to model the hardware circuitry of the second electronic component.

47. (New) A computer readable medium storing at least a first one or more programs executed in a distributed simulation system that comprises a plurality of nodes, each of the plurality of nodes configured to simulate one of a plurality of electronic components of an electronic system under test, wherein the plurality of nodes are configured to communicate during a simulation using a predefined grammar that includes transmit signal message packets, wherein a transmit signal message packet comprises signal values corresponding to electronic signals in the electronic system under test, the electronic signals providing communication between the plurality of electronic components included in the electronic system under test; wherein a first node of the plurality of nodes is assigned a first electronic component of the plurality of electronic components for the distributed simulation, and wherein the first node comprises the first electronic component implemented in hardware circuitry, and wherein the first one or more programs comprise code to interface to the hardware circuitry to provide input signal values received from other nodes of the plurality of nodes to the hardware circuitry and to capture output signal values driven by the hardware circuitry to provide the output signal values to other nodes of the plurality of nodes; and wherein a second node of the plurality of nodes simulates a second electronic component of the plurality of electronic components using a first simulation mechanism that does not include hardware circuitry that implements the second electronic component.

48. (New) The computer readable medium as recited in claim 47 wherein the first simulation mechanism comprises a first simulator and a first model of the second electronic component, and wherein the first one or more programs comprise the first

simulator.

49. (New) The computer readable medium as recited in claim 48 wherein the first model comprises one or more files also stored on the computer readable medium.

50. (New) The computer readable medium as recited in claim 49 wherein the first model is a register-transfer level model of the second electronic component.

51. (New) The computer readable medium as recited in claim 49 wherein the first model is a behavioral level model of the second electronic component.

52. (New) The computer readable medium as recited in claim 49 wherein the first model is a hardware verification language model of the second electronic component.

53. (New) The computer readable medium as recited in claim 49 wherein the first model is described in a hardware description language that supports constructs for verification and an interface to one or more programming languages.

54. (New) The computer readable medium as recited in claim 47 further storing a second one or more programs, wherein the first simulation mechanism comprises the second one or more programs and the second one or more programs, when executed, model the second electronic component.

55. (New) The computer readable medium as recited in claim 54 wherein the second one or more programs are coded in a programming language and compiled for execution.

56 (New) The computer readable medium as recited in claim 55 wherein the programming language is C.

57. (New) The computer readable medium as recited in claim 55 wherein the programming language is C++.

58. (New) The computer readable medium as recited in claim 55 wherein the programming language is a portable, object-oriented language.

59. (New) The computer readable medium as recited in claim 47 wherein the first simulation mechanism includes an emulator configured to emulate the second electronic component using one or more programmable logic devices to model the hardware circuitry of the second electronic component.

60. (New) A method comprising:

simulating an electronic system under test in a plurality of nodes, each of the plurality of nodes configured to simulate one of a plurality of electronic components of the electronic system under test;

wherein the simulating comprises the plurality of nodes communicating using a predefined grammar that includes transmit signal message packets, wherein a transmit signal message packet comprises signal values corresponding to electronic signals in the electronic system under test, the electronic signals providing communication between the plurality of electronic components included in the electronic system under test;

wherein a first node of the plurality of nodes is assigned a first electronic component of the plurality of electronic components for the distributed simulation, and wherein the first node comprises the first electronic component implemented in hardware circuitry, and wherein the simulating further comprises interfacing to the hardware circuitry to provide input signal values received from other nodes of the plurality of nodes to the hardware circuitry and to capture output signal values driven by the hardware circuitry to provide the output signal values to other nodes of the plurality of nodes; and

wherein the simulating further comprises simulating a second electronic component of the plurality of electronic components in a second node of the plurality of nodes using a first simulation mechanism that does not include hardware circuitry that implements the second electronic component.

61. (New) The method as recited in claim 60 wherein the first simulation mechanism comprises a first simulator and a first model of the second electronic component.

62. (New) The method as recited in claim 61 wherein the first model is a register-transfer level model of the second electronic component.

63. (New) The method as recited in claim 61 wherein the first model is a behavioral level model of the second electronic component.

64. (New) The method as recited in claim 61 wherein the first model is a hardware verification language model of the second electronic component.

65. (New) The method as recited in claim 61 wherein the first model is described in a hardware description language that supports constructs for verification and an interface to one or more programming languages.

66. (New) The method as recited in claim 60 wherein the first simulation mechanism comprises a one or more programs which, when executed, model the second electronic component.

67. (New) The method as recited in claim 60 wherein the first simulation mechanism includes an emulator configured to emulate the second electronic component using one or more programmable logic devices to model the hardware circuitry of the second electronic component.